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Analysis of Surface Effects in Semiconductor Nanodevices Modelled by Means of Monte Carlo Simulations

SVMMARY OF THE DOCTORAL THESiS

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CERTIFY that:

The research work presented in this summary, entitled *Analysis of Surface Effects in Semiconductor Nanodevices Modelled by Means of Monte Carlo Simulations*, and written by **Ignacio Íñiguez de la Torre Mulas** to apply for the Doctor degree, has been carried out under their direction at the Electronics Group in the Applied Physics Department of the University of Salamanca.

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INTRODUCTION

In this Thesis we will study semiconductor ballistic devices able to work at room temperature and at millimeter wave frequencies in view of developing digital/analog electronic devices for ultra–fast (Terahertz) data processing. We will exploit ballistic phenomena (and not phase coherence effects) in nanoscaled devices based on AlInAs/InGaAs heterostructures grown by molecular beam epitaxy on InP substrates. This material system ensures high sheet carrier density and high mobility leading to acceptably low device impedances. Using a high Indium content close to 70% in the InGaAs channel, an electron mobility of 15000 cm^2/Vs at room temperature and 2DEG sheet carrier density of $2.5\times10^{12}/cm^2$ has been obtained. A 2D Monte Carlo (MC) simulator,[1,6] containing all the necessary ingredients (accurate scattering models, presence of dielectrics and surface charges, and "arbitrary" geometries) has been used to physically model the ballistic nanodevices. With this method, a good qualitative (and in some cases quantitative) agreement has been found between the results of the simulations and experimental measurements. MC simulations predict excellent high–frequency operation of the nanodevices, in some cases reaching the THz range. However, the intrinsic performance is deteriorated by the influence of parasitic elements associated with the accesses and contacts, especially crosstalk capacitances. Their combination with the high resistance presented by the ballistic channels induces a degradation of the frequency behaviour and, consequently, devices with cut−off frequencies on the THz range have not yet been realized.

In this context, in recent years great efforts have been made to fabricate and characterize new nanometer–sized electronic devices with ingenious geometries, in which electrons fly ballistically guided by shapes, edges or inner obstacles.[7,8] In this

line of research we find devices like four terminal rectifiers[9–14] and T– and Y–shaped three branch junctions[15–43] (TBJs and YBJs), whose operation has been demonstrated by different authors. A nanoscale unipolar rectifying diode, so called Self–Switching Diode (SSD),[44–52] has also been recently proposed. Its operation is based on the opening/closing of a channel due to the accumulation of charges in the surrounding regions. Under certain bias conditions these diodes show a hysteretic behaviour in the *I–V* characteristic which could be used to fabricate memory devices. For this reason it is called Self–Switching Memory (SSM).[53–54] All of these devices exhibit nonlinear effects and could operate at very high frequencies.

The functionalities of these nanodevices are manifold: rectifiers, frequency doublers, phase detectors, logic operations, signal detection, etc. The development of these promising structures is still under investigation. For this reason, it is necessary to continue working in their design to achieve compact circuits with low power consumption and low noise, which will be the reference of the THz Telecommunications (analogue and digital) in a medium term future.[55]

Some theoretical descriptions of the operation of ballistic devices have been proposed,[56–59] always starting from a coherent transport description based on the Landauer–Büttiker formalism.[60,61] Nonetheless, at room temperature, where the applications are actually interesting, the transport could be considered semiclassical (multimode). To confirm this, our group has proposed a numerical method (MC simulator) based on a semiclassical transport description, able to qualitatively reproduce the main features of the ballistic effects measured in basic devices like T– and Y–branch junctions and ballistic rectifiers, thus demonstrating that, at least at high temperatures (T>77 K), coherent transport plays no significant role on the main characteristics of these devices. [62–68]

The first step in the design of ballistic structures is the determination of their optimal geometry. At this level, simulation tools constitute a valuable alternative to the expensive and time consuming test–and–error procedure. In our case, to check the validity of the simulations results (concerning TBJs) we compared the results of our simulations with measurements obtained in devices fabricated at the IEMN (*Institut d'Electronique, de Microélectronique et de Nanotechnologie du Nord*, Lille, France).[70–72]

At high frequencies (several THz), the intrinsic noise generated by the nanodevices becomes a performance limitation, and must be carefully analyzed in order to reduce its level as much as possible. The MC method has some advantages with respect to other traditional models (like drift–diffusion or hydrodynamic) to analyze high–frequency noise in ballistic devices. It incorporates in a naturally way all the microscopic mechanisms at the origin of noise and describes correctly the ballistic or quasiballistic transport taking place inside the nanodevices.

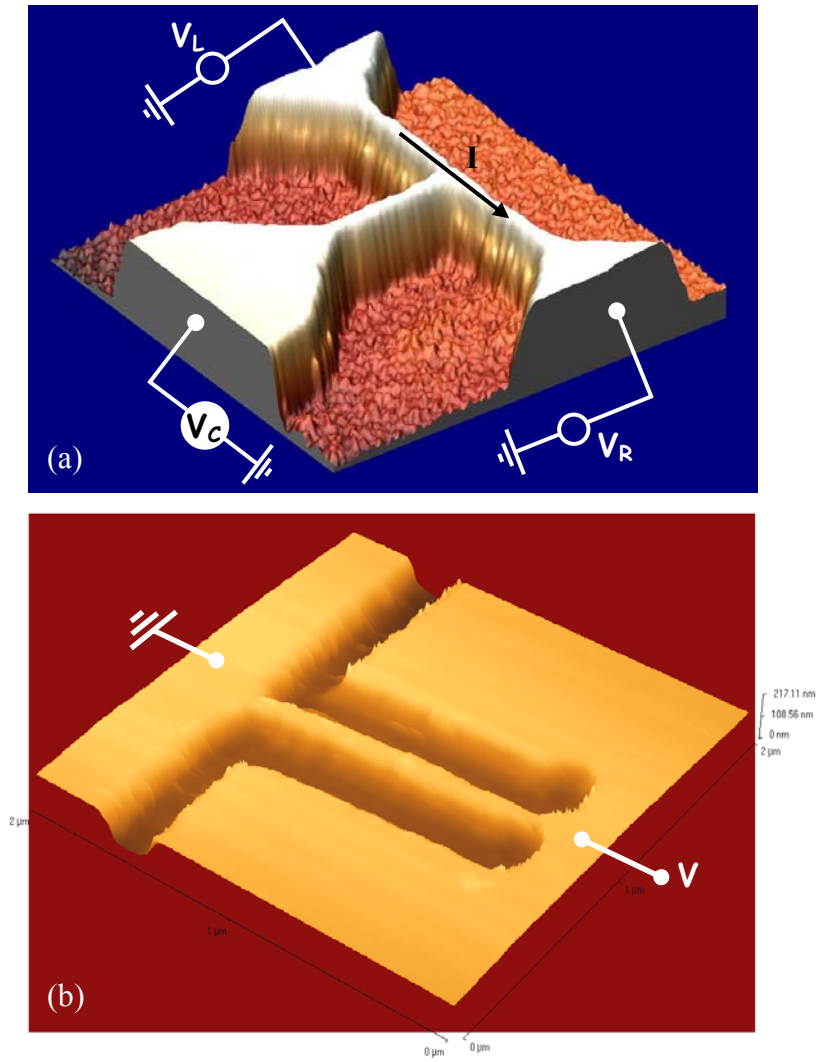

Fig. 1. Atomic force micrographs of a typical (a) TBJ and (b) SSD. Also schematically shown a sketch of the electrical measurement configuration.

At the nanometer scale most of the studies have focused on electron transport properties, while less attention has been paid to surface effects in these nanostructures. As the size of electronic devices is reduced, the surface/volume ratio increases considerably and, in strong contrast to conventional devices, when

dimensions reach the nanometric scale, surface effects can get to have a remarkable importance on electron transport, even becoming decisive in the device behaviour. As it is well known, the origin of surface charge in dielectric/semiconductor interfaces is the rupture of the crystal periodic potential. As a consequence, new states localized at the semiconductor surface with energies within the gap appear and can be occupied by electrons. The role and the influence of this surface charge on the output characteristics will be the main topic under study throughout this work.

In this framework, the aim of the present Thesis is to report on a new model in which the local value of the surface charge is updated self–consistently with the carrier dynamics near the interface during the simulation. This new model is applied to investigate the influence of the surface charges especially on devices like TBJs and SSDs, shown in Fig. 1.

The outline of this summary is as follows. First, in Chapter I we discuss the physical model used for the MC simulation of the ballistic structures. In Chapter II we put special emphasis on the modelling of the surface charge, providing the details of the algorithm, and also of noise calculations. Chapter III is dedicated to examine the dependence of the well–known parabolic behaviour of the output voltage V_C measured at the bottom of the (open circuited) central branch of TBJs on the width of the vertical branch.[73–75] We also study the influence of the size of the horizontal branch. Some results concerning the frequency response are also discussed. In Chapter IV we successfully apply our model to explain the physics of the SSD rectifying behaviour to analyze and discuss the ac and noise spectra dependence on the topology of the devices, providing design indications to improve their performance.[76,77] In some cases the surface states may become very useful for practical applications like in the case of the Self–Switching Memory, that we analyze in Chapter V, where we provide an in depth explanation of its operation in terms of the charging and discharging of the surface states on the etched sidewalls of the structure. Devices with different geometries have been simulated, and a detailed microscopic analysis of the behaviour of surface charge and potential profiles has been performed.[78,79] Finally the main conclusions of the present work are summarized.

I. MONTE CARLO MODEL. METHODOLOGY

We will make use of a semiclassical ensemble MC simulator self–consistently coupled with a 2D Poisson solver. The transport model locally takes into account the effect of degeneracy and electron heating by using the rejection technique and the self–consistent calculation of the local electronic temperature and Fermi level.[80] The surface charges appearing at the boundaries of the semiconductors in contact with dielectrics are also considered in the model.[81] The validity of this approach has been checked in previous works by means of the comparison with experimental results of static characteristics, small signal behaviour and noise performance of a 0.1 μm gate AlInAs/InGaAs lattice matched HEMT (InP based).[81,82] Since contact injection is a critical point when dealing with ballistic transport, the velocity distribution and time statistics of injected carriers will be accurately modelled.[83,84]

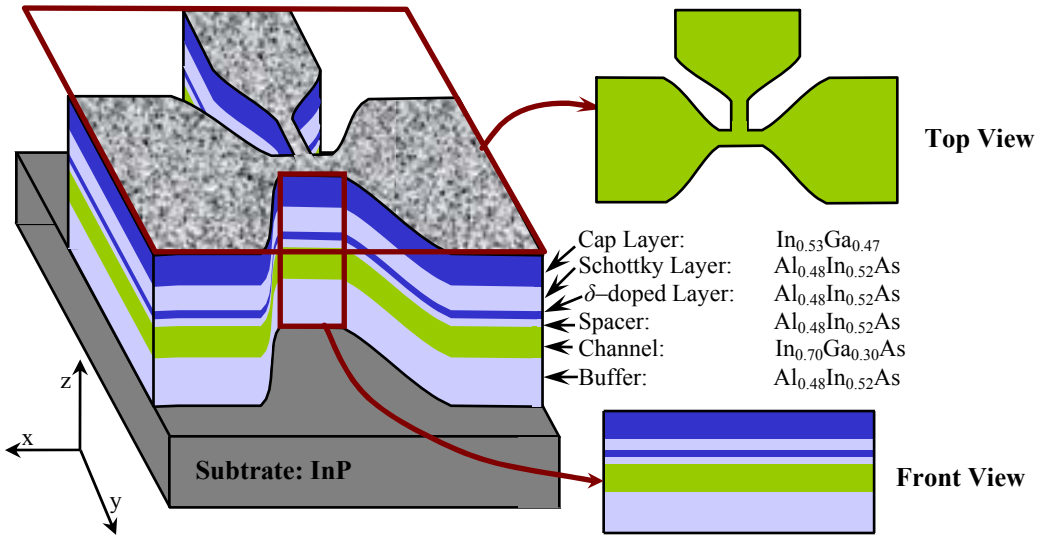

Fig. 2. Three–dimensional (3D) geometry and layer structure of the ballistic channels and scheme of the 2D front–view (FV) and top view (TV) MC simulations.

For the correct modelling of these devices, a 3D simulation would be necessary in order to take into account the effect of the lateral surface charges and the real geometry of the structures. However, for the moment, only a 2D MC model has been developed, and some simplifications and assumptions must be made.[63] To account for the top geometry of the devices (for TBJs, YBJs, or ballistic diodes in our case), TV (top–view) simulations will be carried out (see Fig. 2). They are performed in the *xy* plane; therefore, the real layer structure is not included, and only the InGaAs channel will be simulated. In order to account for the fixed positive charges of the whole layer structure, a net doping N_{db} is assigned to the channel in TV simulations, but impurity scattering is switched off. In this way, the electron transport through the undoped channel is well reproduced, since this is a "virtual" doping N_{db} associated with the charges of the cap and δ–doped layers. On the other hand, a negative surface charge density σ is assigned to the semiconductor–air interfaces to account for the influence of the surface states originated by the etching processes.

Concerning the analysis of noise, in the simulation we follow the standard scheme. The instantaneous current is calculated using the generalized[85] Ramo–Shockley[86,87] theorem, which evaluates the simultaneous contribution of all super particles involved in the MC simulation to the total electrode current. The mathematical quantity employed for the characterization of noise is the autocorrelation function of current fluctuations, $C_I(t)$, defined as:

$$C_I(t) = \lim_{T\to\infty} \frac{1}{T}\int_0^T \delta I(t')\delta I(t'+t)dt'$$

where $\delta I(t)=I(t)-\bar{I}$ is the total current fluctuation around the average value $\bar{I}$ and the bar indicates time average. By the Wiener–Kintchine[88] theorem the autocorrelation function is related to the spectra density as:

$$S_I(f) = 2\int_{-\infty}^{\infty} C_I(t)e^{j2\pi ft}dt.$$

II. SURFACE EFFECTS

SELF–CONSISTENT CHARGE MODEL

The surface–to–volume ratio in nanoelectronic devices increases as the geometries are scaled down, so that the device behaviour is more and more affected by the physical properties of the surfaces. Sidewall surface charge provokes the depletion of part of the conducting semiconductor channel as a consequence of coulombian repulsion and thus lowers the carrier density near the interface with the dielectric. In the total depletion approximation, the depletion width originated by a surface charge σ is $W_d=\sigma/N_{db}$ at each side of the channel. Therefore, the effective conduction width is $W_{eff}=W-2W_d$, with W the total width of the channel. With the aim of extracting the experimental lateral depletion width W_d, the electrical characterization of channels with different length and width has been made. A value of W_d about 40 nm ($\pm$ 10 nm) for $In_{0.7}Ga_{0.3}As$ channels,[89] corresponding to a surface charge density of $\sigma/q=(0.4\pm0.1)\times10^{12}$ cm^{-2} (using $N_{db}=10^{17}$ cm^{-3}), has been obtained near equilibrium conditions.

A simple way to include the influence of this surface charge in MC simulations is to consider a model in which σ is fixed to the experimentally–extracted equilibrium value, and kept constant independently of the topology of the structure, position along the interface, bias and time. This model will be denoted as constant–charge model (CCM). The surface charge is included as a Neumann boundary condition for the Poisson equation: $\varepsilon_2 E_2^n - \varepsilon_1 E_1^n = \sigma$, with ε_i the permittivity and E_i^n the normal electric field in the i–th material. The applicability of this model becomes doubtful when the semiconductor becomes totally depleted (for W lower than 80 nm,

so that W_{eff} becomes negative). Indeed, the physical origin of the surface charges is the trapping of electrons in surface states (located in the middle of the gap), but if the region near the surface is completely depleted, no electron would be able to reach the surface and the surface charge should decrease. In such a case ($W_{eff} < 0$), if the CCM is used, the background doping N_{db} can not compensate the negative surface charge, charge neutrality is not ensured and unphysically high negative potentials are obtained in the simulation, providing incorrect results.

Some features of the surface charges make difficult the possibility to implement them precisely in a MC simulator. The occupation of the surface states depends not only on its energy level but also on the potential profile and the Fermi energy in the surrounding region (these aspects are the base of the recently proposed new concept of nanoscaled memory point, the Self–Switching Memory).[53,54,78,79] Moreover, surface physical and chemical properties, fabrication processes, surface oxidation, composition and roughness determine the properties of the surface states and, as a consequence, the response of nanometer scale devices. In addition, the capture and emission mean times of surface states (with values typically in the μs range) are much higher than scattering times, thus preventing their detailed treatment in a microscopic MC scheme, since a huge CPU–time would be necessary to take into account the correct dynamics of these states. Another possibility to obtain a stationary profile of the surface charge is to solve the trap occupancy and the MC carrier concentration iteratively. Nonetheless, for this sake the properties of the traps (density, cross–section and energy distribution) must be known, and it is not our case. For all these reasons, we have developed a new model, based on the depletion induced by traps and not on their statistics, in which the local value of the surface charge is updated self–consistently with the carrier dynamics near the interface during the simulation.[73] This model completes and improves the previous works where a constant surface charge density (neither depending on the position nor on the applied potential) was considered at the semiconductor–dielectric interfaces associated with the presence of surface states.[62,68] The philosophy of our model, called self–consistent charge model (SCCM), is based on the adaptation of the value of the surface charge to the carrier density in the nearby region. First, we evaluate the carrier concentration for every mesh adjacent to the interface (n_{int}) as an average over a given number of iterations N_i. Then, it is checked if n_{int} has a value in the range

(n_{dis}, n_{char}) with $n_{dis}=N_{db}/50$ and $n_{char}=N_{db}/100$, which represent the limits to which we try to adapt the electron concentration next to the interface. If the concentration (n_{int}) is higher than the upper limit (n_{char}), we increase the surface charge in a given amount $\Delta\sigma=10^{-10}$ cm^{-2}, so that its repulsive effect provokes stronger channel depletion and thus the concentration should diminish. On the other hand if n_{int} is smaller than the lower limit (n_{dis}), the surface charge is decreased in the same density $\Delta\sigma$ to reduce the (too large) induced depletion. The choice of the limits n_{dis}, n_{char} is constrained by the level of statistical resolution achievable by the simulation (which depends on the number of simulated electrons). If the lower limit is too low (the forced depletion level is too strong), below the value of electron concentration that MC simulations can reliably estimate, wrong results would be obtained. N_i=500 has been chosen as a trade–off to optimize the precision of the time dependent electron concentration without much increasing the run–time of the simulation. Neither N_i nor $\Delta\sigma$ influence significantly the final results, though they can eventually modify the time it takes to reach the stationary surface charge profiles.

Till now, we have considered that the physical mechanism that provokes variations of in the occupancy of surfaces states is thermionic emission processes of electrons from/to the channel. Nevertheless, as explained in Ref. 53 for the case of SSMs, this transmission of charge is modulated by the combination of thermionic emission and tunnelling phenomena. In order to consider these phenomena, we have implemented in our MC simulator an improvement of the previous self–consistent charge mode for being able to describe the memory effects found in SSMs.[78,79]

The philosophy of the model is essentially the same, but considering a new magnitude, the perpendicular electric field, to take into account the surface charging via tunnel effect. So, first, the values of $E^{\perp}$ and n_{int} are calculated as an average over N_i iterations. If the electric field $E^{\perp}$ exceeds a "discharging threshold value" E_{dis} and the neighbouring concentration n_{int} is smaller than a "discharging level" n_{dis}, the local value of σ is decreased by $\Delta\sigma$. The field condition reflects the fact that the slope of the conduction band in the channel perpendicular to the interface is sufficiently high (the barrier is thin enough) to have large probability for tunnelling processes which discharge surface states, Fig. 3(a). Moreover, since n_{int} is small, surface state charging processes are negligible as compared to tunnelling charge release. On the other hand, if the perpendicular electric field $E^{\perp}$ is lower than a "charging threshold

value" E_{char} and the carrier density is higher than a "charging level" n_{char}, the dominating mechanism is the filling of surface states by thermionic emission, and σ is raised in the same quantity $\Delta\sigma$, Fig. 3(b). In the cases in which the electric field and the free carrier concentration do not fulfil these conditions, situations sketched in Fig. 3(c), charge trapping and release are considered to be negligible or approximately compensate each other and the value of σ is kept constant. Since the electric field is the slope of the potential barrier existing between the surface states and the channel, the threshold values E_{dis} and E_{char} could be connected with the activation energy of the surface states and the barrier width, as shown in Fig. 3(d). The higher the activation energy, the higher the slope of the conduction–band necessary to attain a barrier thin enough to have a significant probability of electron tunnelling into the channel.

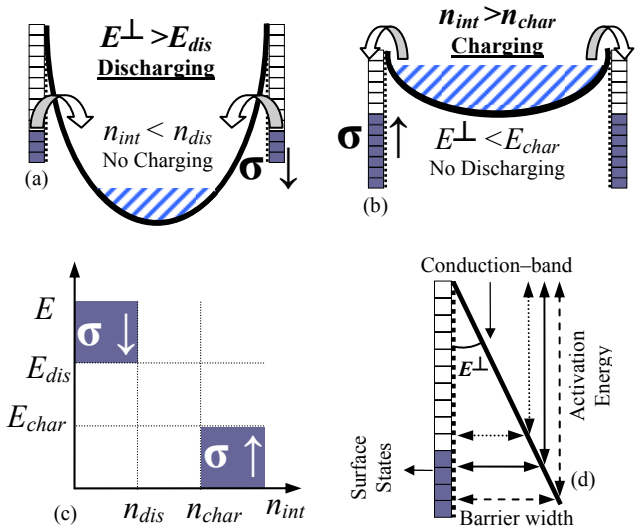

Fig. 3. Sketch of the conduction–band profiles in the channel for different bias voltages: (a) discharging of surface states by tunnelling into the channel, and (b) charging of surface states by thermionic emission from the channel. (c) Scheme of the different conditions considered in the surface charge algorithm. (d) Illustration of the relation existing among the activation energy of the surface states, the perpendicular electric field and the barrier width.

To conclude, it is important to remark that evidently this "ad–hoc" surface charge model is not able to reproduce the statistics of occupation of surface states, but it does describe correctly the global effect of the surface charge. We will apply this self–consistent model to study TBJs and SSDs based on InAlAs/InGaAs layers and compare the results with experimental measurements, achieving a satisfactory agreement.

III. T–BRANCH JUNCTIONS

We analyze the influence of the surface charge on the output voltage V_C measured at the bottom of the (open circuited) vertical branch of T–shape three–terminal ballistic junctions fabricated with different widths of the vertical branch W_{VER}. The new self–consistent model, in which the local value of the surface charge is dynamically adjusted depending on the surrounding carrier density, is used in the calculations. The rectifying behaviour exhibited by these devices (down–bending shape of the output voltage V_C as a function of the push–pull applied voltage $V=V_R=-V_L$) is found to be much influenced by the surface charge. A satisfactory agreement is achieved between simulated results and experimental measurements.

Previous works[15,30,63] show that when electron transport is ballistic and TBJs are biased in push–pull fashion, V_C is found to be always negative (as long as $V\neq 0$), whereas if transport is diffusive one would expect simply $V_C=0$ regardless of the input potential. The basic operation of TBJs has been explained in terms of space charge effects originated by the joint action of surface charges at the semiconductor/air interfaces and inhomogeneous charge distributions associated with the ballistic motion of carriers along the channel.[90] Simulations[63] and experiments[15,30] showed that V_C is a quadratic function of V for small applied potentials, as predicted in Ref. 57. We have found that this well known behaviour is much influenced by the surface charges in both the horizontal and vertical branches. With the help of experimental measurements performed in real devices, the influence of the width of the vertical branch on the values of V_C and its relation with surface charge effects are studied.

The fabrication process and experimental characterization of the TBJs have been carried out in the IEMN. The layer structure, grown by molecular beam epitaxy

(MBE), consists of an InP substrate, a 200–nm $Al_{0.48}In_{0.52}As$ buffer followed by a 15–nm $In_{0.70}Ga_{0.30}As$ strained channel, three layers of $Al_{0.48}In_{0.52}As$ (a 5–nm spacer, a δ–doped layer, and a 10–nm Schottky layer), and finally, a 15–nm $In_{0.53}Ga_{0.47}As$ cap layer. The geometry of the TBJs was defined by a high resolution negative e–beam resist, Hydrogen Silses Quioxane (HSQ), exposed by a LEICA EBPG5000+ machine, and $CH_4/H_2/Ar$ Reactive Ion Etching (RIE).[70–72,89] Then Ni–Ge–Au–Ni–Au metals were evaporated and annealed to form ohmic contacts and, finally, Ti–Au bonding pads were realized.

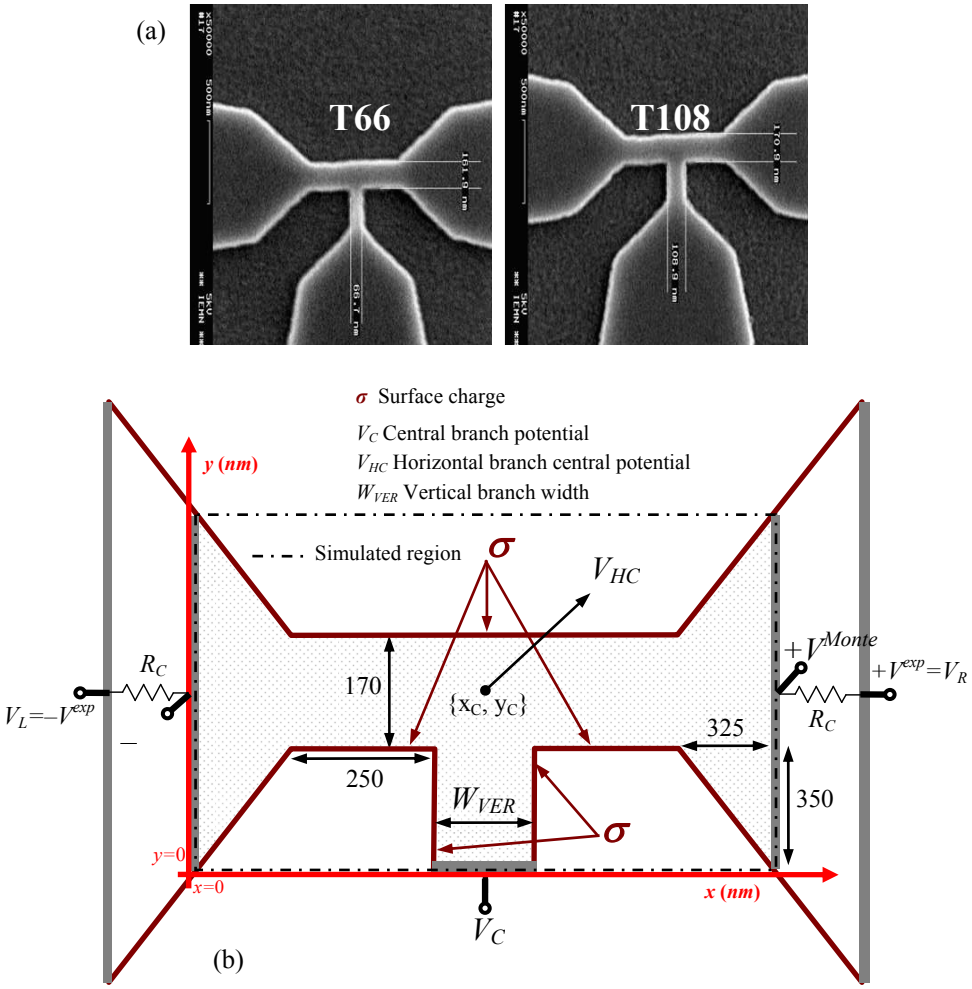

Fig. 4. (a) SEM images of the TBJs with 66 and 108 nm wide vertical branches. They will be denoted as T66 and T108 respectively. (b) Schematic representation of the simulated T–Branch Junctions. Lengths of the accesses, horizontal and vertical branches are indicated in nm.

Five TBJs with different widths of the vertical branch, W_{VER}=66, 78, 84, 94 and 108 nm, have been fabricated. Scanning electron microscope (SEM) images of the TBJs with 66 and 108 nm wide vertical branches are shown in Fig. 4(a). For our MC analysis we consider the geometry shown in Fig. 4(b). The voltage V_C is

calculated by averaging the electric potential (and subtracting the equilibrium value) at the bottom of the (open circuited) central branch. We will also show results for the value of the electric potential at the centre of the horizontal channel, which will be denoted as V_{HC}.

Fig. 5(a) shows the experimental values of the potential V_C in the central branch (measured with a high–impedance voltmeter) and the current I flowing through the horizontal branches in the TBJs when biased in push–pull fashion. The parabolic behaviour of V_C is strengthened when reducing the width of the vertical branch, which means that T66 generates higher (negative) values of V_C. This is in principle an unexpected result, since the vertical branch was believed to be only a measure (passive) element,[62,63] in such manner that the value of V_C should be independent of its width W_{VER}. The inset of Fig. 5(a) shows how, as expected, the current is independent of W_{VER}, since the horizontal branch is practically identical for the different TBJs.

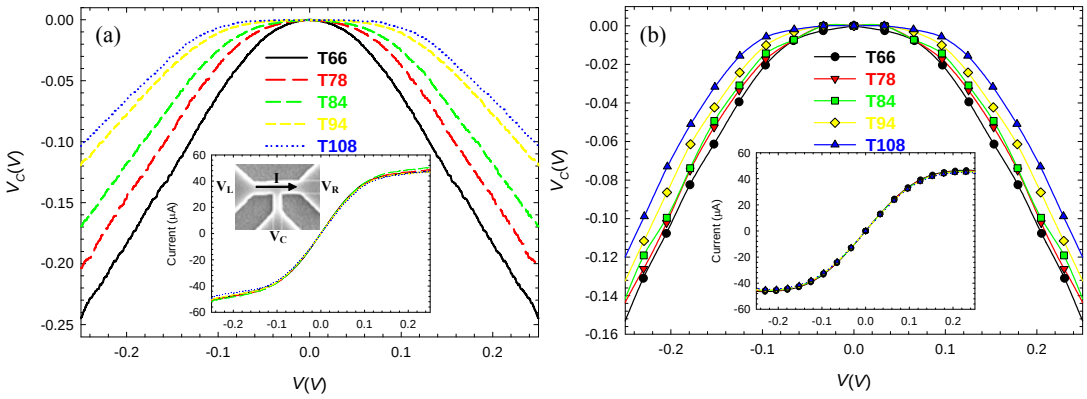

Fig. 5. (a) Experimental and (b) MC values of the bottom potential V_C and current (insets) in the TBJ junctions with 66, 78, 84, 94 and 108 nm wide vertical branches (denoted as T66, T78, T84, T94 and T108, respectively) as a function of the push–pull bias V.

We have tried to reproduce these measurements with MC simulations using the CCM for the surface charge with $\sigma/q=(0.4\pm0.1)\times10^{12}$ cm^{-2} ($W_d \approx 40$ nm), the results being totally in disagreement with experiments. In contrast, the calculations of V_C shown in Fig. 5(b), performed with the SCCM, are consistent with the experimental results, showing the same trend and a satisfactory quantitative agreement. The agreement is excellent for the TBJs with the wider vertical branches (T94 and T108). When W_{VER} is decreased, the simulated V_C–V curves, while following the same trend as measurements (higher negative values for lower W_{VER}, with quadratic shape at low

bias), do not increase their parabolicity as much as in experiments. Finally, concerning the current, insets of Fig. 5(a) and Fig. 5(b), the agreement is totally satisfactory for the whole set of junctions, both qualitatively and quantitatively. Let us try to understand the previous results by means of the information provided by MC simulations. Firstly, we remark that the proposed SCCM allows for the variation of the surface charge σ along the position in the interface in accordance with the surrounding free carrier concentration. This possibility of self–adaptation allows the surface charge in the narrowest junction (T66) to reach values that approximately cause total depletion of the vertical branch, $\sigma/q=0.3\times10^{12}$ cm^{-2}, Fig. 5(a). In contrast, in the widest junction (T108) the surface charge is limited by a value close to that obtained in the experimental measurements, $\sigma/q=(0.4\pm0.1)\times10^{12}$ cm^{-2}.[89] These facts support the physical consistency of our model. Furthermore, the surface charges take a value practically constant near the bottom of the vertical branch, which indicates that the results will not change if this branch is made longer, Fig. 6(a).

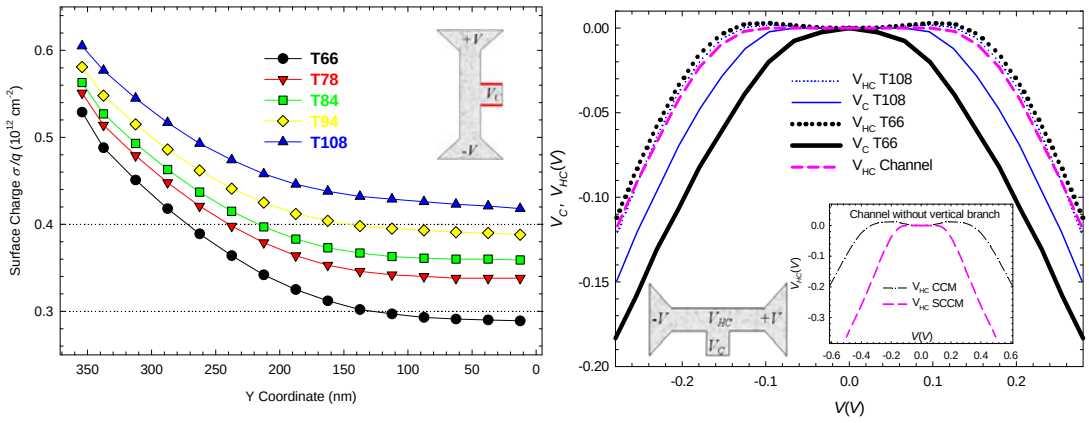

Fig. 6. (a) Surface charges in the sidewalls of the vertical branch under equilibrium conditions (V=0). (b) V_{HC} and V_C as a function of the applied voltage for the TBJs with W_{VER}=66 and 108 nm. V_{HC} for a channel without vertical branch is also plotted for comparison. The inset shows V_{HC} calculated in the channel without vertical branch with the CCM ($\sigma/q=0.4\times10^{12}$ cm^{-2}) and SCCM models of surface charge.

In previous works (using the CCM for the surface charges)[62,63] the vertical branch was considered as a voltage probe, providing at its bottom (V_C) the variations of V_{HC} (potential at the centre of the horizontal branch). However, within the SCCM, the surface charge in the sidewalls of the vertical branch and the carrier penetration inside it change with the bias (like in Y–Junctions),[63] which provokes that V_C is no longer a faithful reflection of the V_{HC} variations and it is necessary to consider the

electric potential difference ΔV_V between V_C and V_{HC}. Therefore, the values of V_C can be considered as the result of two combined effects: a horizontal one (given by V_{HC}) and a vertical one (given by ΔV_V).

We analyze first the horizontal effect, that is, the values of V_{HC}. In Fig. 6(b) we plot the values obtained with the MC simulations for V_{HC} in T66 and T108, together with those calculated in a channel without vertical branch. It can be observed that, as expected, the values of V_{HC} practically coincide in the three structures (transport takes place in horizontal direction and the width and length of the horizontal branch are practically the same). The inset of Fig. 6(b) also compares the values of V_{HC} in a simple channel (without vertical branch) obtained with the CCM and SCCM models of surface charge. The SCCM leads to a considerable increase of the negative values of V_{HC}, which is the signature of an enhanced charge asymmetry in the horizontal direction. Such an asymmetry appears in the concentration profile, especially for high values of V, for which a strong depletion of carriers takes place at the anode side of the horizontal branch. This region becomes highly resistive, so that most of the applied potential drops here and leads to the high negative values of V_{HC}. The presence of ballistic transport in the horizontal direction produces the same qualitative effect,[62,63,90] but weaker than that observed here, thus originating smaller negative values of V_{HC}, like those obtained with the CCM, inset of Fig. 6(b). This interesting phenomenon, the strong carrier depletion near the anode taking place for high V, is caused by the high surface charge present in this zone of the device. The origin of the increase of the surface charge with the applied voltage near the anode lies in the fact that, due to the ballistic motion of electrons, their longitudinal energy increases significantly as they approach the right contact. Scattering mechanisms, even if there are very few, produce some energy redistribution, and thus make the transversal energy component also increase. In this way electrons are able to approach the boundaries of the TBJ (in spite of the repulsive effect of the surface charge) and contribute to raise the value of σ. As expected, this effect is more important for higher V.

In view of the previous results we can conclude that the dependence of V_C on the width of the vertical branch W_{VER} is associated with the changes in the vertical profile of the electrostatic potential (ΔV_V) among the different TBJs, since V_{HC}, accounting for the horizontal effects, does not depend on W_{VER}. When the structure is

biased, the potential difference with respect to the equilibrium case at the bottom of the central branch, providing the measured electric potential V_C, is higher for T66 than for T108. This explains the increasing negative values of V_C versus V obtained as W_{VER} is reduced, Fig. 5. With the SCCM the difference of the electrostatic potentials with respect to the equilibrium case varies along the vertical branch, in contrast with the constant separation provided by the CCM,[63] where the vertical branch could be considered as a voltage probe not influencing the values of V_C.

Apart from the fitting of the measurements performed in the TBJs with different W_{VER} fabricated at the IEMN, our surface charge model can also be applied to explain the experimental behaviour found in similar TBJ structures, recently reported in the literature,[32] where the length L^{HOR} and the width W^{HOR} of the horizontal branches are modified. When the length of the horizontal branches L^{HOR} is changed we found that the values of V_{HC} are very similar for all the structures. This is due to the analogous horizontal concentration profiles found for the different lengths. As in the previous TBJs, it is the presence of the vertical branch and the associated surface charges which induce different values of V_C in each of the structures. Like in the case of the experimental results reported in Ref. 32 we find that the down–bending behaviour of V_C is stronger for shorter junctions. This result is expected because of the more ballistic character of transport in shorter structures, but our results indicate that surface charges and the presence of the vertical branch also play a role. Concerning the width of the horizontal branch W^{HOR} the values of V_C are higher (more negative) as the width is decreased, in accordance with the trend found in experiments.[32] Remarkably, and in contrast with the behaviour found when modifying W_{VER} and L^{HOR}, in this case the values of the potential at the centre of the junction V_{HC} exhibit a strong dependence on W^{HOR}. In these structures, despite the length is the same, the profile of carrier concentration along the horizontal branch depends strongly on W^{HOR} due to the depletion induced by the surface charges. As expected, carrier concentration at the centre of the horizontal branch is lower for smaller W^{HOR} due to the more pronounced depletion so that the electric potential and consequently the values of V_{HC} changes significantly with W^{HOR}. Such differences are smoothed along the vertical branch by the influence of surface charges, but are still noticeable at its bottom, in the values taken by V_C.

With the aim of improving the dynamic behaviour of the TBJs, structures with wider horizontal branches (500 nm) have been simulated and experimentally measured, thus to diminish their resistance (paying the price of loosing sensitivity given by the smaller values of V_C). In these junctions the adaptation of the surface charge (at the laterals of the horizontal branch) with the bias is irrelevant, so that the negative values of V_C are essentially caused by a vertical effect, originated by the self–adjustment of the surface charge and electron concentration in the vertical branch.

Concerning the frequency response, in the low frequency region (<MHz) mixing measurements have been done. For low amplitudes of the applied signals (<0.25 V), and as a consequence of the quadratic response, the fundamental harmonic of the original frequencies, the sum and the difference frequencies, as well as the dc (direct current) component are found. For higher amplitudes new harmonics appear due to the non–parabolic shape of the output voltage V_C.

We have also checked the capability of TBJs to work at very high frequencies. The intrinsic behaviour predicted by MC simulations shows that the three–terminal junctions work as frequency doublers up to 100 GHz and as rectifiers even at THz. Experimentally, phase detection and frequency doubling have been measured up to 4 GHz.

IV. SELF–SWITCHING DIODE

By tailoring the boundaries of a narrow semiconductor channel to break its symmetry, in 2003 A. M. Song *et al.*[44] proposed a new type of nanometer–scale nonlinear device, called Self–Switching Diode (SSD). The key point in the fabrication of the device is the etching of the insulating grooves that appear in Fig. 1(b) as dark areas. An applied voltage V not only changes the potential profile along the channel direction, but also either widens or narrows the effective channel depending on the sign of V. This results in a diode–like characteristic, but without the use of any doping junction or barrier structure. The turn–on voltage can be widely tuned from virtually zero to more than 10 V, by simply adjusting the channel width. The two–terminal structure of the SSD allows SSD–based circuits to be realized by a simple single step lithographic process, so that its size can be easily reduced to the nanometer–range. Thus, by using fast III–V materials, the high frequency performance of SSDs can be dramatically boosted thanks to a much shorter transit time, due not only to a smaller channel length but also to an enhanced electron velocity associated to ballistic transport. Moreover, the possibility of combining N SSDs in parallel allows to overcome the important problem (when trying to reach ultra high frequency operation) of the high input resistance of the discrete devices, also providing an improvement of the signal–to–noise ratio by a factor of $\sqrt{N}$.[47,52] And last but not least, the planar geometry of the SSDs allows placing the two contacts with long separation, so that parasitic crosstalk capacitances can be drastically reduced. These facts, together with the intrinsically high electron velocity of InGaAs channels, should permit the fabrication of SSDs working in the THz range.

By means of our semiclassical 2D MC code described in Chapter I, we have analyzed the static, dynamic and noise behaviour of InAlAs/InGaAs–based submicron SSDs.[76,77]

The voltage applied to the anode (right contact) of the SSD propagates to the vicinity of the channel, while in the cathode region (at the left of the trenches) the potential is always essentially zero. In equilibrium, the channel is closed due to the depletion induced by the surface charges located at the lateral walls, which lead to the appearance of a longitudinal potential barrier. When $V>0$, the positive voltage reaches the lateral regions of the SSD channel, so that the potential barrier is lowered (or even removed), thus allowing the electron flow (the channel is open). On the contrary, when $V<0$, the potential profile in the right part of the device is almost unchanged with respect to the equilibrium situation (it is just shifted to lower values), the channel thus remaining closed. Therefore, the operation principle of this device is similar to that of an enhanced mode field effect transistor (pinched off at equilibrium) in which lateral gates (in this case short circuited to the drain) control the current flow through the channel. From the point of view of applications, the non–linear response of the diodes and the ultra fast ballistic transport opens the possibility of fabricating circuits for harmonic generation at very high frequencies.[52]

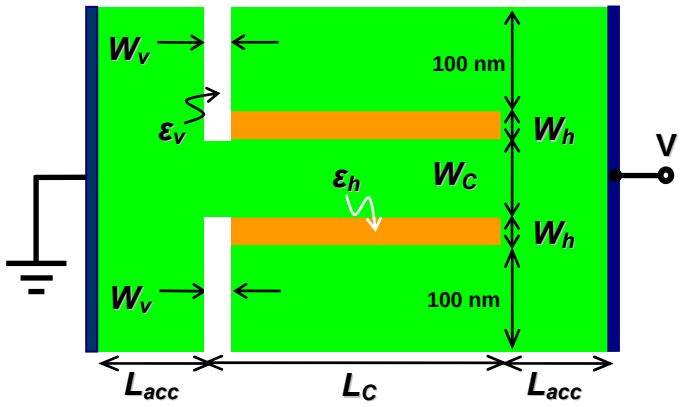

Fig. 7. SSD geometry.

We have analyzed the *I–V* characteristics (Fig. 8) when some parameters of the diode geometry are modified (keeping the others constant): (a) channel width W_C, (b) channel length L_C, (c) and (d), horizontal and vertical width of the trenches W_h and W_v, respectively, and (e) and (f) permittivity of the material in the horizontal and vertical trenches ε_h and ε_v, respectively. The reference SSD for all the simulations will be the one with: W_C=50 nm, L_C=250 nm, W_h=W_v=5 nm, ε_h=ε_v=1 and L_{acc}=175

nm (see Fig. 7). In order to optimize the current control of SSDs, we have reduced the width of the trenches to 5 nm (near the limits of up–to–date technology), so that the potential applied to the right contact affects more strongly the population of the channel.

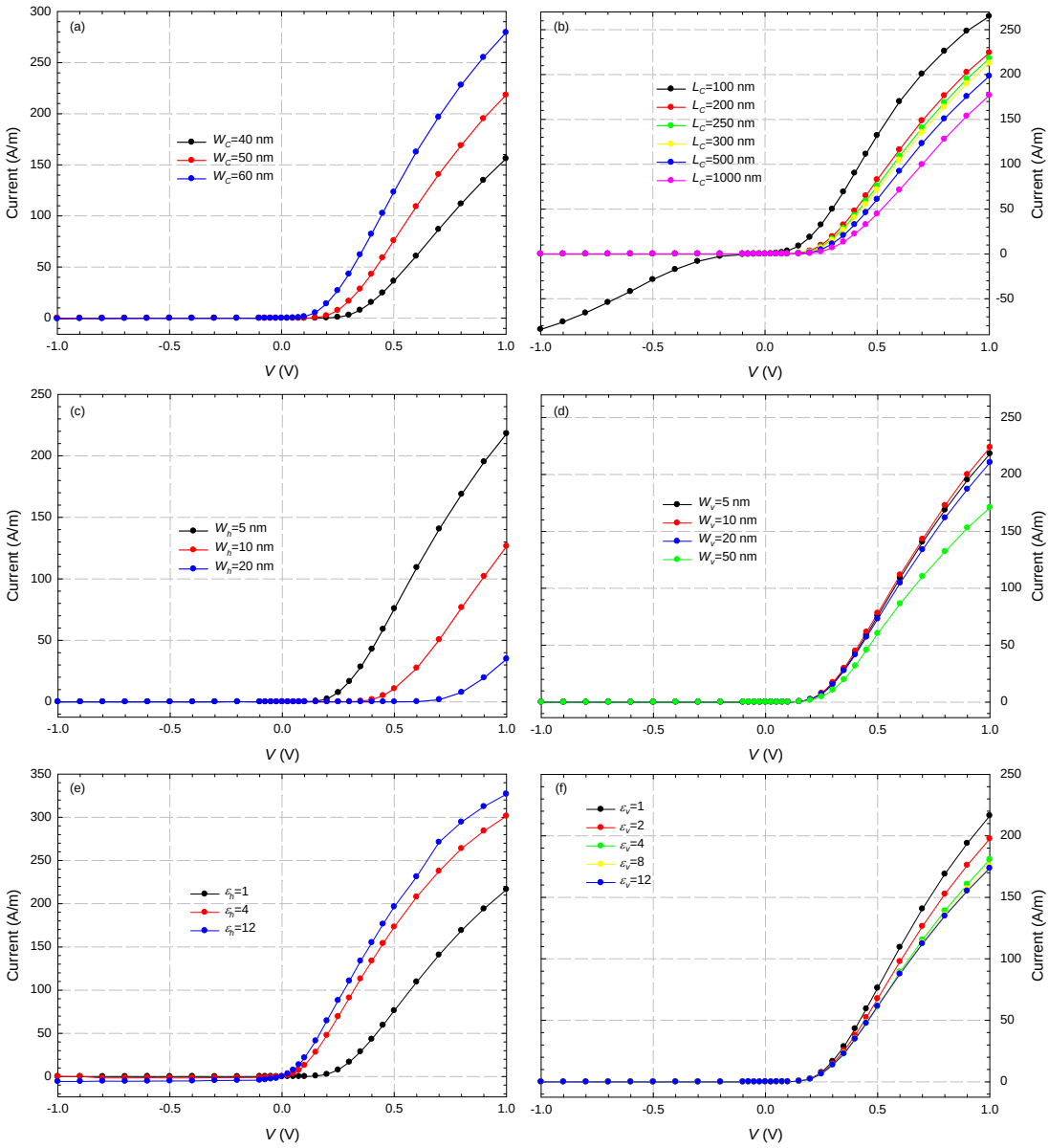

Fig. 8. *I–V* curves of the SSDs with different (a) W_C=40, 50 y 60 nm, (b) L_C=100, 200, 250, 300, 500 y 1000 nm, (c) W_h=5, 10, 20 nm, (d) W_v=5, 10, 20 y 50 nm, (e) ε_h=1, 4 y 12 and (f) ε_v=1, 2, 4, 8 y 12.

The longitudinal profiles of electric potential along the centre of the device show a barrier for the electron motion induced in the channel by the charge at the surface states. This barrier controls the current flow in both directions. Due to the asymmetry of the diode, the barrier is lowered much more by forward than by reverse applied biases, thus providing the rectifying behaviour typical of SSDs,

which is observed in the *I–V* curves of Fig. 8. The forward current shows an exponential dependence on the applied voltage for low values of *V* (as long as the barrier is present), and then becomes linear (resistive behaviour), with a tendency to saturation at the highest applied voltages due to hot–carrier effects.

For devices with a smaller channel width W_C, Fig. 8(a), the turn–on voltage is larger due to a larger barrier at equilibrium, which needs a higher applied voltage to disappear. The length of the channel, L_C, is also found to largely influence the device behaviour. As observed in Fig. 8(b), short–channel effects appear when the aspect ratio of the channel (L_C/W_C) decreases. In such a case, under reverse bias, the potential of the lateral regions is not able to deplete the channel, so that the barrier preventing the current flow disappears and an inverse leakage current flows (as observed for L_C=100 nm). The very thin trenches of the devices not only prevent the presence of inverse leakage current for very short channels (it only appears for L_C=100 nm), but also the forward current is much improved, Fig. 8(c). As observed in Fig. 8(c) and Fig. 8(d), the turn–on voltage is influenced by the width of the horizontal (and not by the vertical) trenches, decreasing for smaller W_h. This is due to the stronger transverse electric field present for smaller W_h, which enables a more efficient control of the opening and closing of the nanochannel when biasing the anode. The *I–V* characteristics are similar when modifying the width of the vertical trench, except for the wider one, where the current decreases due to the shorter length of the channel affected by the transverse electric field (the vertical trench is enlarged while keeping constant the total channel length). When increasing the dielectric permittivity of the filling material of the trenches, Fig. 8(e) and Fig. 8(f), we find a similar effect than when decreasing of the width of the trenches. From the point of view of applications it is important to remark that horizontal trenches filled with a high–k material lead to an increase of the current.

The dynamic behaviour of optimized devices can be tested by means of the simulation of their response to sinusoidal input voltage signals, $V(t)=V_0\text{sen}(2\pi ft)$, of increasing frequency. We have studied the time–dependent current in SSDs for different lengths, L_C. For 100 GHz, the rectification is quite good, nearly following the static behaviour. When increasing the frequency of the applied signal, the shape of the current is degraded and a dephase in the response appears, but still showing a positive average value. The mean value of the current is represented in Fig. 9 as a

function of the frequency of the periodic input voltage (V_0=0.25 V) for SSDs with the geometry shown in Fig. 7 when modifying some or their geometric parameters. As a general feature, a peak is observed in the dc response just before its decay. The optimization of the device geometry can provide a maximum rectified current as high as twice the value at low frequencies, which could be useful for providing some frequency selectivity in detection applications. Furthermore, we emphasize the presence of negative values beyond the cut–off frequency (defined as the first zero crossing of the dc current).

As expected, the cut–off frequency of the rectifying behaviour of SSDs depends on the channel length L_C, Fig. 9(a), being lower for longer channels. The SSD with L_C=100 nm is correctly responding up to frequencies over 2.0 THz, thus making possible the operation of these devices as, for example, power detectors of THz waves. We also observe that the maximum of the rectified dc current is sensitive to the properties of the vertical trench, width W_v [Fig. 9(c)] and permittivity ε_v [Fig. 9(e)], but insensitive to that the horizontal trenches, W_h [Fig. 9(b)] and ε_h [Fig. 9(d)].

To understand the origin of the peak in the dc response, a model based on the time–dependent charging and discharging of the region close to the vertical trench has been recently proposed by the group of A. M Song.[91] When the SSD is biased, the regions surrounding the channel will be charged or discharged, which results in the opening or closing of the nanochannel. To characterize these phenomena, we study the time–dependence of a parameter Δ defined as

$$\Delta = \frac{N_{db} - n(f)}{N_{db} - n(0)}$$

with $n(f)$ and $n(0)$ the carrier concentration for a frequency f and at equilibrium (V=0 V), respectively, in the region within 50 nm at the right sidewall of the vertical trenches. With this definition, when Δ>1 the trench sidewall is positively charged (channel opened) with respect to equilibrium conditions, and if Δ<1 there are more negative charges (channel closed).

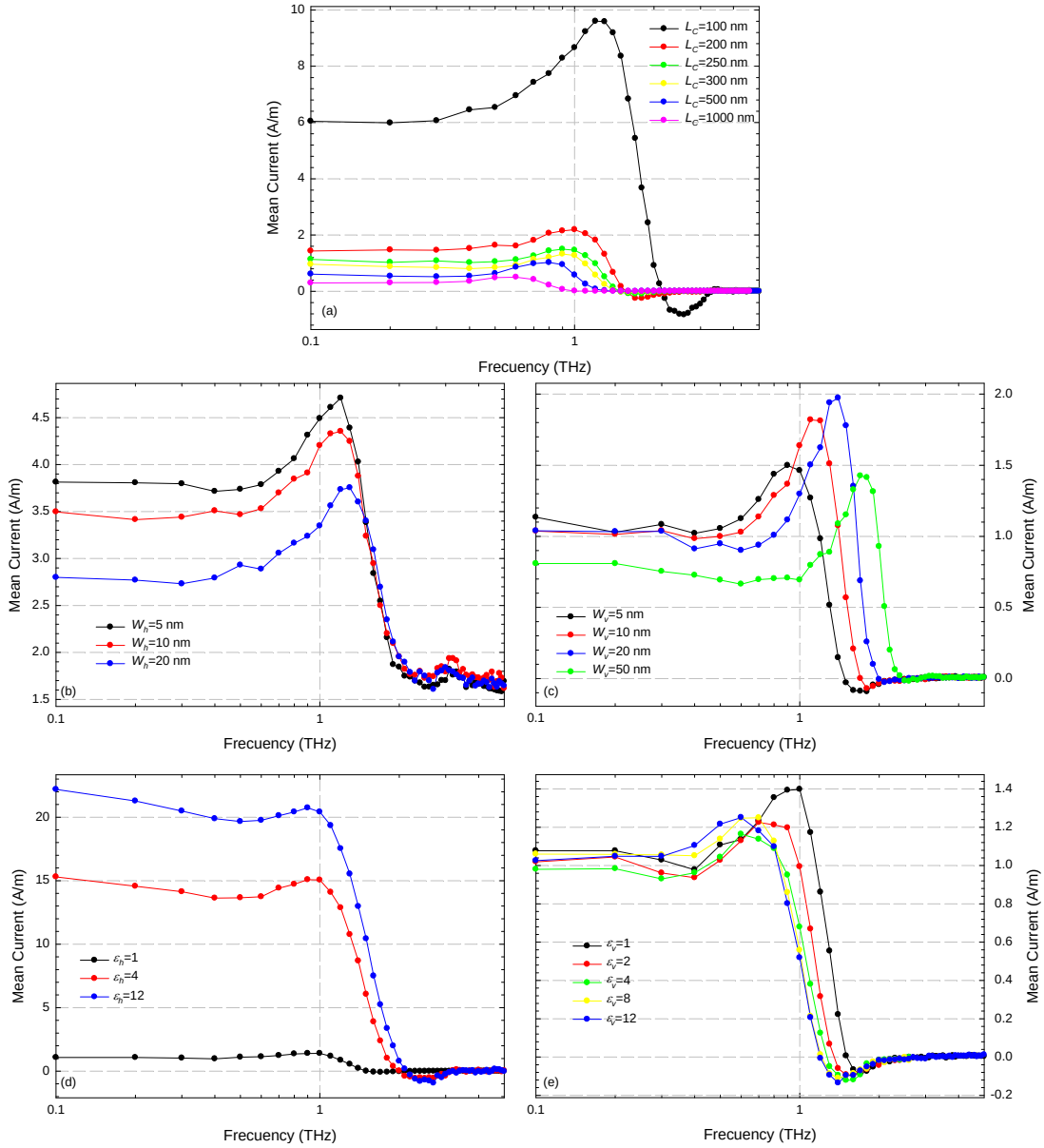

Fig. 9. Mean response current to a periodic input voltage (with amplitude of 0.25 V) applied to the SSDs of Fig. 7 *vs* frequency. (a) L_C=100, 200, 250, 300, 500 y 1000 nm, (b) W_h=5, 10, 20 nm, (c) W_v=5, 10, 20 y 50 nm, (d) ε_h=1, 4 y 12 and (e) ε_v=1, 2, 4, 8 y 12.

The frequency dependence of the phase shift $\delta\varphi$ between Δ and the electric potential dropped in the nanochannel, together with a resonance in the charging/discharging of the region surrounding the channel, provide the explanation of the peak in the rectification. This model perfectly explains all the dependencies of the frequency response of the rectified current. For example, the rectified current is zero when $\delta\varphi = \pi/2$ and takes negative values when $\delta\varphi > \pi/2$. Finally, the peak in the response is originated by a resonance between the frequency of the applied voltage and the characteristic frequency of the charge oscillations in the region near

the vertical trench (whose origin will be explained later), which leads to a peak in the amplitude of Δ. It is also worth noting that the position of the maximum shifts to lower frequencies as ε_v is increased, but exhibiting a saturation for ε_v=4. This effect will be explained later.

By downscaling the device dimensions, the operation frequencies of SSDs can reach the THz range at room temperature,[76,77] as experimentally demonstrated in Ref. 46,47 for an array of these devices working as detector up to 110 GHz. At so high frequencies, the intrinsic noise generated by the diodes becomes a performance limitation, and must be carefully analyzed in order to reduce its level as much as possible. By means of our semiclassical 2D MC simulator we have analyzed the current noise spectra of submicron SSDs.[92]

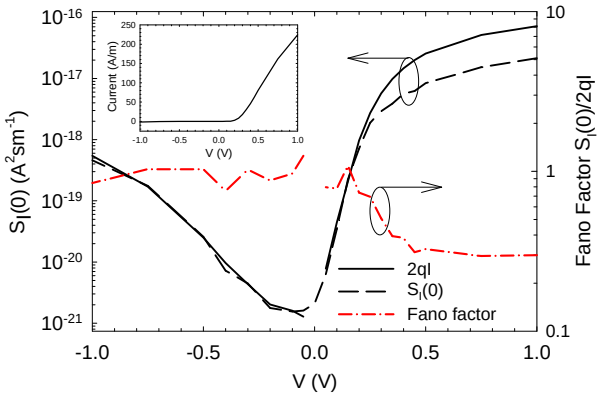

Fig. 10. MC values of $S_I(0)$, compared to $2qI$, as a function of the applied voltage (left axis). The Fano Factor $S_I(0)/2qI$ is also plotted (right axis). The inset shows the I–V curve of the diode in linear scale. Reference SSD: L_C=250 nm, W_C=50 nm, W_h=W_v=5 nm, ε_h=ε_v=1 and L_{acc}=175 nm.

Fig. 10 reports the values of the spectral density of current fluctuations in the reference SSD at low–frequency (in the plateau beyond the $1/f$ range) $S_I(0)$ compared to the $2qI$ value (with q the electron charge). The corresponding Fano Factor F=$S_I(0)/2qI$ is also shown. As long as the barrier limiting the current level has a significant value (higher than about 0.1 eV, approximately $4k_BT$ at room temperature, with k_B the Boltzmann constant), the SSD displays full shot noise (both under forward and reverse bias), which indicates that transport is barrier controlled and the current is provided by uncorrelated carriers surpassing the barrier. At high forward bias the barrier is lowered or even disappears, the channel resistance decreases, and the diffusive accesses to the channel become more and more important in the total noise of the device. Thus, $S_I(0)$, which now essentially corresponds to diffusion noise in the series resistance, shows an increasingly

suppressed value with respect to full shot noise (F<1). In contrast, in the reverse bias range shown in Fig. 10 the barrier persists and full shot (F=1) noise is always obtained. This is the typical noise behaviour exhibited by SSDs as long as transport in the channel is ballistic or quasiballistic.

We have also calculated the equivalent noise temperature of the diode $T_n=S_I(0)R/4K_B$ as a function of the forward current. R is the low–frequency incremental resistance of the SSD, calculated from the slope of the I–V curve. T_n is an important parameter used to experimentally characterize the noise properties of diodes.[93–95] At low currents, corresponding to the exponential region of the I–V characteristic, the noise temperature is close to half the value of the lattice temperature, $T_n=T_{300}/2$. This is a feature associated with an ideal exponential dependence of the forward current on the applied voltage [$I \propto \exp(qV/K_BT_{300})$], which usually goes along with the previously commented full shot–noise behaviour, $S_I(0)=2qI$. As the current increases, the effect of the thermal noise in the series resistance becomes important (the channel resistance decreases exponentially), and the noise temperature increases towards the lattice temperature (T_{300}=300 K). Once the barrier disappears, a strong electron heating takes place and the noise temperature increases significantly over the lattice temperature. This behaviour of the noise temperature is quite similar to that found in other barrier–controlled devices, like Schottky barrier diodes,[93–95] except in the very sharp increase observed once the barrier disappears, which is more pronounced in SSDs.

Fig. 11 shows the current noise spectra $S_I(f)$ corresponding to different bias conditions in the reference SSD. In order to identify the influence of the field fluctuations on the total noise, calculations performed when the Poisson Solver (PS) is switched off in the simulations (an average electric field profile previously obtained with the PS on is adopted instead) are also shown for an applied voltage of 0.2 V.[95] Two main peaks are observed in the spectra. Plasma oscillations are at the origin of the one appearing at the highest frequencies (above 3 THz).[96] Stemming from electric field fluctuations coupled to the carrier movement, plasma oscillations are not present if the PS is switched off, and the associated peak disappears. The other peak, at around 1.3 THz, is attributed to returning–carrier effects taking place in the space–charge regions originated by the surface charge at both sides of the vertical trenches. As seen in the inset, which shows the frequency dependence of

$S_I(f)$ in log–log scale for V=0.0 V, it exhibits the characteristic f^2 behaviour already found in other devices like Schottky–barrier diodes,[93,95] revealing a capacitive coupling of the returning carrier fluctuations to the noise at the terminals. When switching off the PS, this peak does not disappear; it is shifted to lower frequencies and increases in amplitude. As expected, with and without PS the spectral density takes the same value at low frequency, corresponding to full shot noise associated with the electrons surpassing the barrier and reaching the anode. At high current levels (V=0.3 V in Fig. 11), a significant enhancement of low frequency noise extending to higher frequencies takes place.

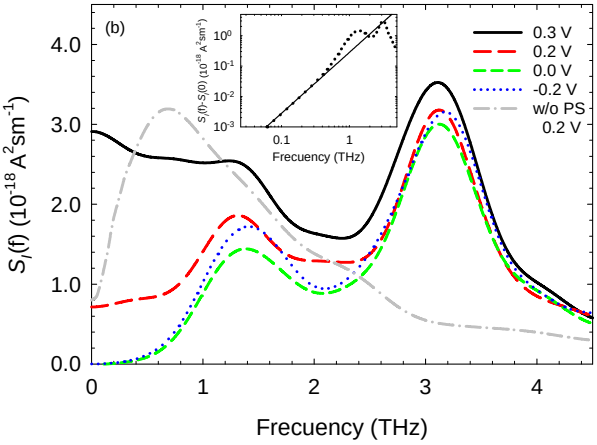

Fig. 11. $S_I(f)$ for several bias conditions in the reference SSD. The case in which the PS switched off is also shown for V=0.2 V. The inset illustrates the f^2 dependence of the noise spectrum for V=0.0 V.

Fig. 12 shows the noise spectra obtained from MC simulations when modifying some or the geometric parameters of the reference SSD (keeping the others constant). As observed, the level of noise at high frequency is higher the larger is the impedance of the accesses as compared to that of the channel. This explains, for example, why $S_I(f)$ is higher when decreasing L_C or increasing W_C or L_{acc}, while it remains with similar amplitude when changing W_h, W_v, ε_h or ε_v. The increase of $S_I(f)$ originated by the peak at lower frequency could limit the frequency range of potential SSD applications. Thus, a first possibility to reduce the noise related to the returning–carriers peak is to decrease the resistance of the accesses relative to that of the channel. The best choice to this end is to shorten L_{acc} [see Fig. 12(g)], which is always desirable to reduce parasitic resistances but may increase the parasitic capacitance between electrodes. Decreasing W_C, Fig. 12(a), or increasing L_C; Fig. 12(b), would enhance the channel resistance and reduce the current level, both undesirable effects. Moreover, a longer channel leads to lower cut−off frequency.

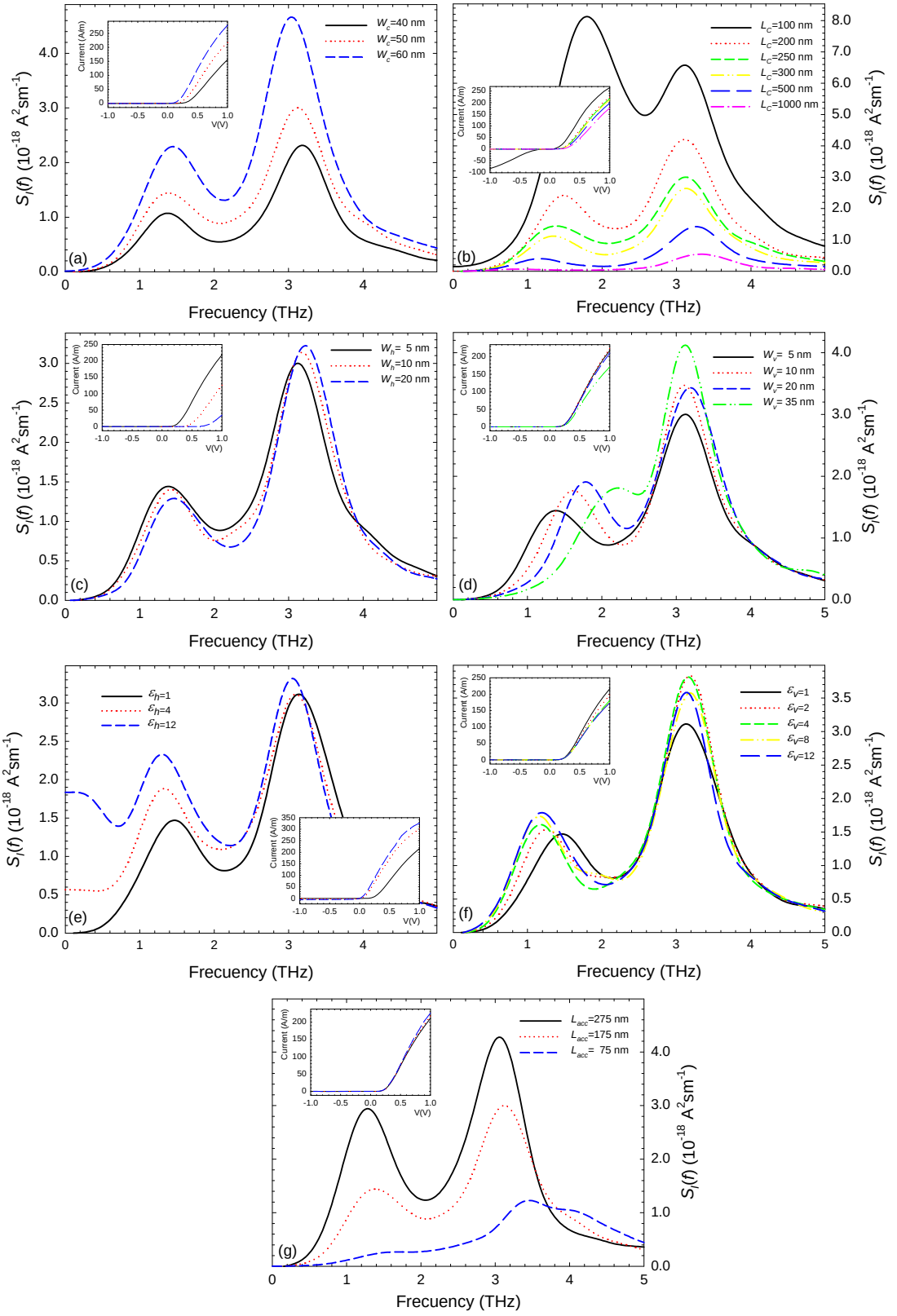

Fig. 12. Current–noise spectra at equilibrium when some parameters of the topology of the diode are modified: (a) W_C=40, 50 y 60 nm, (b) L_C=100, 200, 250, 300, 500 y 1000 nm, (c) W_h=5, 10, 20 nm, (d) W_v=5, 10, 20 y 50 nm, (e) ε_h=1, 4 y 12, (f) ε_v=1, 2, 4, 8 y 12 and (g) length of the accesses L_{acc}=275, 175, 75 nm. The insets show the corresponding *I–V* characteristics.

A second possibility is to try to move the peak to higher frequencies, thus reducing the amplitude of the noise in the range of interest (around 1 THz). As observed in Fig. 12, by modifying W_C, L or L_{acc}, the frequency of the maximum hardly changes. In contrast, an increase in the width of the vertical trenches W_v, Fig. 12(d), or a decrease of its permittivity ε_v, Fig. 12(a), shifts the peak to higher frequencies, Fig. 12(f). Let us explain this behaviour. The origin of the low frequency peak is related to the dynamics of the reflected carriers (returning carriers) in the region close to both sidewalls of the vertical trenches, which capacitively couple to the current at the terminals. This coupling is modulated by two capacitors, one associated to the depletion regions at both sides of the trenches, C_{ZCE}, and the other due to the vertical trenches themselves, $C_v=\varepsilon_v/W_v$ (that is why the effect of ε_v and W_v in the low frequency peak is totally opposite).

When comparing the results shown in Fig. 9, corresponding to the dynamic response of the rectified current, and in Fig. 12, related to the noise spectra, it is noticed that the behaviour of the low frequency peak and its relative amplitude is very similar in both cases. This indicates that, quite probably, we are observing the same microscopic phenomenon reflected in different macroscopic quantities. It means that the charge fluctuations close to the vertical trench reflect themselves both in the noise spectra (charge at both sides) and in the dc mean current (mainly charge at the right sidewall, coupled to the channel via the horizontal trench). It must be beard in mind that that the spectral density at equilibrium is proportional to the small signal admittance of the device, whereas the dc response current is caused by the diode rectification and corresponds to large signal conditions. Moreover, the rectified current is phase shifted by the horizontal capacitor, while the noise is only influenced by the vertical one (with no need of the presence of a conducting channel). All these facts explain why the frequency of the peak does not coincide exactly in both quantities.

The physical origin of the maximum in the rectified current has also been analyzed in Ref. 91, where this peak is attributed to non–dispersive localized surface plasma (LSP) oscillations, like those observed in metal–insulator–metal (MIN) structures.[97] This explanation is compatible with ours (in terms of returning–carriers) taking as a basis the theory presented in Ref. 93, on the noise behaviour in Schottky–barrier diodes. This reference shows that the characteristic frequency of the

returning–carriers movement is proportional to the bulk plasma frequency of the material, indicating that their dynamics is closely connected to plasma oscillations.

The results discussed so far moved us to modify the geometry of the diode in the region around the vertical trenches in order to reduce the noise in the THz range. In this line, SSDs with the vertical trench tilted with an angle ϕ have been simulated. For ϕ=45º we have obtained a significant reduction in the noise at frequencies around 1–2 THz as compared with the reference SSD, where ϕ=90º. The rectified current also shows a significant shift (around 600 GHz) of the resonant peak to higher frequencies.

Finally, we propose an equivalent circuit (EC) that allows providing a qualitative interpretation of the noise spectra in terms of the frequency dependence of the diode impedance $Z(f)$; $S_I(f)=4K_BT\mathrm{Re}[Y(f)]$ at equilibrium. R–L–C circuits are used in regions where transport is diffusive (accesses to the channel), while the channel, where transport is expected to be ballistic or quasiballistic, is represented by an R–C circuit. Finally, the geometrical capacitance associated with the vertical trenches $C_v=\varepsilon_v/W_v$ and the capacitances associated to the depletion regions C_{ZCE} are also included. The parameters involved in each of the sub–circuits of the global EC can be either determined from the diode geometry or estimated from the results of MC simulations. With this equivalent circuit, we have been able to reproduce the shift of the low frequency peak towards higher frequencies (and thus the decrease of the noise in the range of interest for applications) when the vertical trench is widened. Also, the saturation in the shift of the low frequency peak when increasing ε_v has been explained as a consequence of the series combination of C_v and C_{ZCE}, so that the equivalent capacitance is fixed by the lowest one. When ε_v is increased to the limit in which C_v becomes much higher than C_{ZCE}, the equivalent capacitance is practically C_{ZCE}, so that the position of the low frequency peak is unchanged.

The last section of this chapter of the Thesis is dedicated to briefly analyze the operation of new devices and circuits based on SSDs, such as Self–Switching Transistors (SST), logic gates and silicon–based SSDs.

V. SELF–SWITCHING MEMORY

Usually, sidewall surface states cause undesirable effects on electron transport and may drastically influence the device output characteristics. For this reason, surface or interface traps in a nanostructure are considered as a problem to avoid or eradicate. Nonetheless, in some cases these surface states may become very useful for practical applications.[44,53,67] This is the case of the Self–Switching Memory (SSM) device recently proposed by A. M. Song *et al*.[44] The geometry of the device is the same as that of a SSD. If the applied voltage remains within certain range, the *I-V* curve of the SSM is independent of the voltage sweep direction. However, when the applied voltage is higher than a certain threshold, both in negative and positive voltage sweep, a well–defined hysteresis loop appears which can be exploited for memory applications. Here, by means of our semiclassical MC simulator, we study the hysteresis effects taking place in the rectifying current–voltage characteristic of the diode.

With the help of the self–consistent charge model (SCCM)[73] with the improvement described in Chapter II we have simulated InGaAs SSMs at 300 K with the geometry shown in Fig. 7 (with W_c=60 nm, L_C=250 nm, W_h=W_v=10 nm, ε_h=ε_v=1 and L_{acc}=175 nm) and different discharging threshold fields E_{dis} (always with E_{char}=20 kV/cm), Fig. 13(a).[78,79] By means of the microscopic quantities provided by the MC simulator we can provide an explanation for the hysteresis effects in terms of the population of the surface states at the channel sidewalls. Fig. 13(b) shows the average surface charge density at the sidewalls of the channel. A maximum value of σ/q=0.5×10^{12} cm^{-2} is allowed, corresponding to a total occupation of the surface states. The voltage sweep starts from 2.0 V, when the surface states are fully occupied, and then follows the direction of the arrows. When

decreasing V down to 0.0 V, the current takes the same values for the different E_{dis} because the surface charge remains essentially constant, as observed in Fig. 13(b). When going to negative voltages, the sidewall surface charge significantly decreases, thus allowing the current flow (let us remind that for values lower than $\sigma/q \approx 3.0\times10^{15}$ m^{-2}, for which $W_d \approx W_c/2$ the channel is open). The higher the value of the discharging field, the higher the negative threshold voltage necessary to release the surface charge and allow the current flow. Additionally, the reverse current level also decreases for higher E_{dis} due to the larger amount of surface charge remaining in the surface states for a given applied voltage, Fig. 13(b).

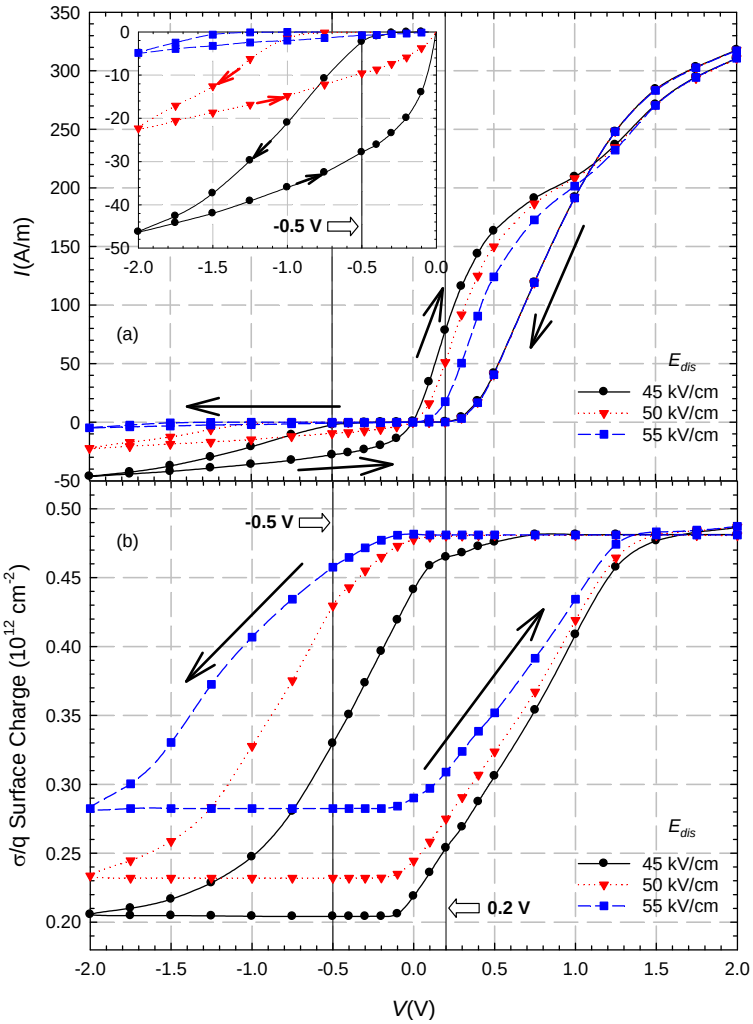

Fig. 13. (a) I–V curves of SSMs with different E_{dis}. The inset shows a zoom of the reverse bias loop. (b) Average value of surface charge in the sidewalls of the channel.

When sweeping the voltage upwards from V=–2.0 V, the surface charge does not change until a significant number of electrons fill the channel and $n_{front}>n_{char}$, situation that is only reached when a positive bias is applied. In contrast with the downwards sweep, the direct current now is different for each E_{dis}, since, even if the

evolution with V is similar, the initial value of the surface charge is not the same. An interesting feature appears at around V=+1.0 V, where the upward and downward I–V curves exhibit a crossover, also found in the experimental measurements.[53]

From the evolution of the current with the surface charge it becomes clear that if the reverse applied voltage is not enough to empty the surface states, the device I–V curve will correspond to the standard rectifying behaviour of a typical SSD,[67] and no hysteresis loop will be found. Such a hysteresis effect can be used for memory applications. Two different binary memory states can be clearly distinguished both for +0.2 V and –0.5 V. The switch between both memory states can be performed by applying a ±2.0 V pulse (+2.0 to set a "1" and –2.0 V to set a "0"), and the reading by +0.2 V or –0.5 V test pulses.

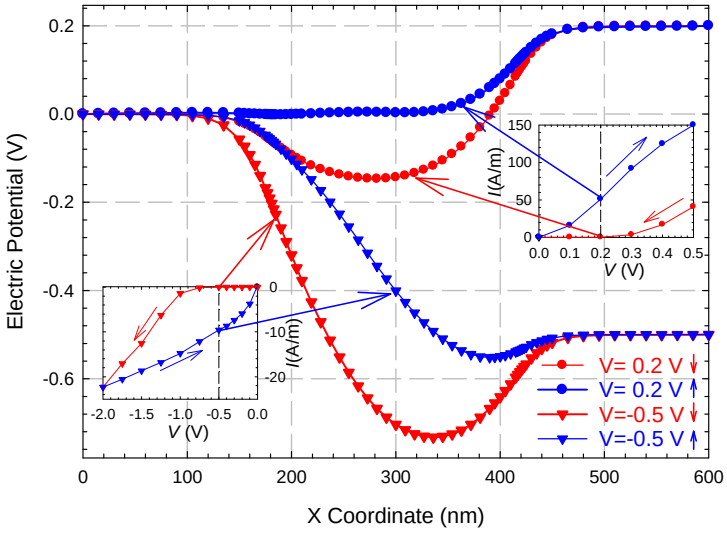

Fig. 14. Profiles of electric potential along the channel for different bias conditions. The inset shows the I–V characteristic in forward and reverse bias. E_{dis}=50 kV/cm.

In order to better understand the hysteresis loop and the different memory states, Fig. 14 shows the electric potential along the channel inside the SSM with E_{dis}=50 kV/cm for different bias points (indicated in the inset). For V=+0.2 V, if the voltage is sweeping downwards from +2.0 V, when the surface states are almost totally filled, the potential profile shows a pronounced barrier for the electron movement in both directions (channel closed). On the contrary, when the states have not yet been charged (upwards sweep), the potential barrier for the electrons moving from left to right is removed, allowing the electron flow. Similar results are found for V=–0.5 V, after the discharging of the surface states (arriving at –2.0 V and

sweeping up); the right–to–left barrier practically disappears, allowing a nonzero value of the reverse current.

In order to optimize the memory operation, we have simulated SSMs where the width W_C and the length L of the channel are varied. The thinner the channel, the higher the negative bias needed to achieve hysteresis. Similarly, the positive threshold voltage needed to switch on conduction is higher when the channel is narrowed. Concerning the length, the current in longer channels is smaller (due to the higher impedance) and hysteresis phenomena in the reverse region are less pronounced, exhibiting a higher threshold voltage. As a general behaviour, when the aspect ratio (L_C/W_C) is decreased, the potential barrier limiting the electron flow is smaller, so that the discharging condition of the sidewall states is reached for lower bias (soft hysteresis loop) and a significant reverse current flows.

CONCLUSIONS

A semiclassical MC simulator has been used to physically model ballistic nanodevices and to analyze surface–charge effects. We have developed a self–consistent model in which the local value of the surface charge is updated dynamically according to the carrier concentration in the nearby region. Since the nonlinear behaviour observed in some of the nanostructures is related to electrostatic effects, these surface charges may play a significant role, and their modelling can be especially critical in the regions of the devices near to be completely depleted. This method has been proved to be useful to predict the behaviour of the devices when operating at room temperature. Even if some of the analysed structures would require a 3D simulator, the 2D MC technique we have used, by introducing some simplifications and assumptions in the model, is able reproduce most of the experimental findings observed at room temperature. Qualitative (and in some cases quantitative) agreement has been found between the results of the simulations and experimental measurements. Once validated, the MC technique has been used to optimise the design of the ballistic structures in order to improve their performance. MC simulations predict excellent high–frequency operation of the nanodevices, in some cases reaching the THz range. However, the intrinsic performance is expected to be deteriorated by the influence of parasitic associated with the accesses and contacts.

The main conclusions obtained in this work can be summarized as follows

- **T–Branch Junctions**

The influence of surface charge phenomena on the behaviour of nanometer scale TBJs has been analyzed. The results of the simulations have been favourably compared with experimental measurements of devices fabricated at the IEMN.

Higher negative values are obtained for V_C as the widths of the vertical branch W_{VER} is decreased. We have found that V_{HC} is nearly independent of the width of the vertical branch, and even of the presence or absence of this branch. Therefore, the dependence of V_C on W_{VER} comes from a vertical effect originated by the microscopic processes taking place inside the vertical branch. Due to the bias dependence of the surface charge and electron concentration within this branch, the variations of V_{HC} are not transmitted in the same way to the bottom of the vertical branch when its width is modified. Indeed, an increasing negative value of V_C is found when reducing W_{VER} due to the total depletion of this branch. This effect can be used to improve the sensitivity or the output power in practical applications of the TBJ, such as power detection or frequency doubling (associated with the characteristic quadratic dependence of the output voltage on the bias, $V_C=-\alpha V^2$).

A strong increase of the depletion near the anode of the TBJs is obtained with the self–consistent surface charge model (due to the increase of energy related to quasiballistic electron transport), thus enhancing the asymmetry of the electron concentration. As a consequence, the values of the potential at the centre of the horizontal branch V_{HC} calculated with the SCCM model are significantly higher than those obtained with the CCM.

The influence of the length and width of the horizontal branches has also been analyzed with our simulations and found to agree qualitatively with experimental findings. The wider the width of the horizontal branch, the lower the (negative) values obtained for V_C. This behaviour can be understood in terms of surface charge effects and depletion of the horizontal branch. The same outcome, less pronounced down–bending, has been obtained increasing the length of the horizontal branch. This result is expected because of the more ballistic character of transport in shorter structures, but our results indicate that surface charges and the presence of the vertical branch also play a role.

- **Self–Switching Diodes**

Modifications of the geometry (width or length of the channel, width or permittivity of the insulator trenches) allow controlling the current level and the turn–on voltage: the wider the channel or the horizontal trenches, the higher the threshold voltage. In order to increase the current level, we need a shorter channel or thinner horizontal trenches (optimally filled with a high–k material). On the contrary,

the capacitance of the vertical trenches should be reduced (wide trenches or filled with low permittivity materials) in order to obtain the best HF performance of the SSDs.

A certain degree of frequency selectivity in the rectifying operation of SSDs could be achieved thanks to the presence a resonant peak in the frequency response whose position can be tuned by modifying the geometry of the SSD. This resonance is originated by charge oscillations taking place in the region close to the vertical trenches.

As regards the current noise spectra, at low frequency shot–noise originated by carriers randomly surpassing the barrier present in the channel is found for the lowest currents, when transport is barrier limited. At higher currents, diffusion noise related to the series resistance becomes dominant. At high frequency, two peaks are found in the spectra. The high frequency peak is associated with bulk plasma oscillations. The one at around 1 THz (with a similar origin than the peak in the dc response: returning carriers at the sidewalls of the vertical trenches) is especially problematic for potential applications of SSDs. We have studied how to reduce the noise in this frequency range by modifying several parameters of the device geometry. The best options are decreasing the length of the access regions or increasing the width of the vertical trenches. This is due to the decrease of the capacitance associated with the trenches, which couples the fluctuations originated by the returning carriers at both sides of the trenches to the current at the terminals. Finally, an equivalent circuit able to reproduce qualitatively the noise spectra in terms of the device impedance has been proposed.

- **Self–Switching Memory**

By means of the improved self–consistent surface charge model, based on threshold values of electric field (normal to the interface) and carrier concentration (in the vicinity of the surface) to increase/decrease the density of charge trapped in the surface states, we have provided a MC interpretation of the operating principle of SSMs. The memory effect has been related to the threshold–like voltage dependence of the sidewalls surface charge occupation, controlling the conductance of the channel. The influence of the geometry of the SSMs on the memory operation has also been analyzed.

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